REMARKS

Claims 1-33 are pending in the present application. By virture of this response, claims 1, 12, and 23 have been amended. Accordingly, claims 1-33 are currently under consideration. Amendment and cancellation of certain claims are not to be construde as dedication to the public of any of the subject matter of the previously presented.

Claim Rejection under 35 U.S.C. § 103

Claims 1-33 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Tcherniaev et al. (U.S. Patent No. 6,577,992, herein after Tcherniaev) in view of Zhou et al.(U.S. Patent No. 6,807,520, herein after Zhou). Applicants respectfully traverse these rejections.

With respect to independent claims 1, 12, and 23, Applicants submit that the combination of the Tcherniaev and Zhou references does not teach or suggest each and every element of these independent claims. Specifically, the combination of the Tcherniaev and Zhou references does not teach or suggest at least the following elements of the independent claims 1, 12, and 23:

> storing the group circuits in a scheduled event queue in accordance with priority in time which the group circuits need to be simulated;
>
> retrieving from the scheduled event queue a set of group circuits for simulation within a predetermined time period;
>
> distributing the set of group circuits into a set of predefined event lists, wherein each of the predefined event list stores one or more group circuits of a corresponding event type; and
>
> simulating the one or more group circuits in each of the predefined event list in accordance with a rate of change of signal conditions of each individual group circuit. (Emphasis added)

First, neither the Tcherniaev reference nor the Zhou reference teaches or suggests the claim element of prioritizing the simulation of the group circuits in a scheduled event queue. The Tcherniaev reference teaches a method for generating a hierarchical representation of a circuit using a Min-cut algorithm to include a plurality of subcircuits. Once the hierarchical representation is

generated, it may be used during simulation of the circuit to reduce the number of computations required. The Zhou reference teaches a method for identifying a group circuit for simulation in a hierarchical environment using a "Cut Node" technique on subcircuits to form their corresponding Thevenin Equivalents for computation. In the embodiments disclosed by both Tcherniaev and Zhou, they simulate the group circuits one at a time, but do not teach or suggest the method of storing the group circuits in a scheduled event queue in accordance with priority in time which the group circuits need to be simulated, and they do not teach or suggest the use of the scheduled event queue to manage the simulation events.

Second, neither the Tcherniaev reference nor the Zhou reference teaches or suggest the claim element of distributing the set of group circuits into a set of predefined event lists. In other words, neither of the cited references teaches the concept of categorizing the group circuits for simulation according to their corresponding event types. Such event types provide additional information to the simulator during simulation regarding the different characteristics of the events. Claim 2 and its corresponding supporting descriptions in the specification provide examples of the different event types utilized by the simulator during the simulation, namely an active event list, an isomorphic event list, and an adaptive event list.

Third, neither the Tcherniaev reference nor the Zhou reference teaches or suggests the claim element of simulating the one or more group circuits in each of the predefined event list in accordance with a rate of change of signal conditions of each individual group circuit. Applicants agree with the Examiner that "[A]although Tcherniaev et al. does [not] clearly state the term rate of change of signal, he teaches a simulation over certain period of time and obtain node voltages at specific time," but Applicants submit that the function of "simulation over certain period of time and obtain node voltages at specific time" may also be performed by a conventional SPICE simulator, which the Applicants have disclosed in the background section of the specification. However, Applicants disagree that "Zhou et al. substantially teaches the term change of signal" in Figure 9 and its description as cited by the Examiner. As described in steps 415 to 470, Zhou teaches a method that gets a single event (step 415), which is defined as a change of signal value. Zhou then teaches identifying and grouping leaf cells (step 425), identifying cut nodes (step 430),

computing the Thevenin Equivalent circuit of the group of leaf cells (step 440), simulating the group of leaf cells using the Thevenin Equivalent circuit (steps 450 and 460), and repeating the above steps with the next event (step 470). Zhou is silent about using the rate of change of signal conditions during the simulation of the one or more group circuits in each of the predefined event list.

With respect to claims 2, 13, and 24, Applicants submit that neither the Tcherniaev reference nor the Zhou reference teaches or suggests the concept of categorizing different event types as captured in the claim limitation of a set of predefined event lists, which include an active event list, an isomorphic event list, and an adaptive event list.

With respect to claims 4, 15, and 26, Applicants cannot find in either Tcherniaev or Zhou reference the claim element of "each group circuit stores an event time for indicating priority in time the group circuit need to be solved, and wherein all leaf circuits in the corresponding group circuit share the same event time." The Tcherniaev and Zhou references are silent about prioritizing events for simulation. Because of this, they are also silent about having all leaf circuits in the corresponding group circuit share the same event time.

With respect to claims 5, 16, and 27, as discussed above in claim 1, neither the Tcherniaev reference nor the Zhou reference teaches or suggests the concept of managing simulation of the one or more group circuits with a scheduled event queue. Instead, in the embodiments of these references, they teach simulation of one event at a time. Thus, these cited references are silent about keeping track of the global accepted time and local current time during the simulation of the one or more group circuits. Such elements are required by claims 5, 16, and 27 of the present application.

For at least the reasons presented above, Applicants respectfully submit that the combination of the Tcherniaev and Zhou references does not teach or suggest each and every element of the independent claims 1, 12, and 23. Applicants also assert that claims 2-11, 13-22, and 24-33, which variously depend from their independent claims, are allowable for at least the reason that they depend from allowable independent claims.

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CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. **188122002000**. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: August 28, 2006

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